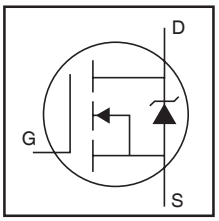
International
IOR Rectifier

PD - 97125

IRF1018EPbF
IRF1018ESPbF
IRF1018ESLPbF

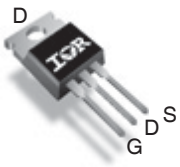
HEXFET® Power MOSFET

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

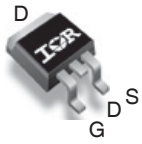


V_{DSS}	60V
$R_{DS(on)}$ typ.	7.1mΩ
max.	8.4mΩ
I_D	79A

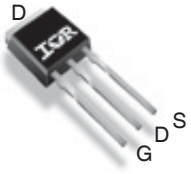
Benefits
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability



TO-220AB
IRF1018EPbF



D^2Pak
IRF1018ESPbF



TO-262
IRF1018ESLPbF

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	79	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	56	
I_{DM}	Pulsed Drain Current ①	315	
P_D @T_C = 25°C	Maximum Power Dissipation	110	W
	Linear Derating Factor	0.76	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	21	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300	
	(1.6mm from case)		
	Mounting torque, 6-32 or M3 screw ⑨	10lb·in (1.1N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	88	mJ
I_{AR}	Avalanche Current ①	47	A
E_{AR}	Repetitive Avalanche Energy ④	11	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	1.32	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface , TO-220	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ⑧	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D^2Pak ⑦⑧	—	40	

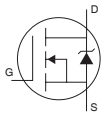
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.073	—	V/°C	Reference to 25°C, I_D = 5mA①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	7.1	8.4	mΩ	V_{GS} = 10V, I_D = 47A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 100µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 60V, V_{GS} = 0V
		—	—	250		V_{DS} = 48V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	110	—	—	S	V_{DS} = 50V, I_D = 47A
Q_g	Total Gate Charge	—	46	69	nC	I_D = 47A
Q_{gs}	Gate-to-Source Charge	—	10	—		V_{DS} = 30V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	12	—		V_{GS} = 10V ④
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	—	34	—		I_D = 47A, V_{DS} =0V, V_{GS} = 10V
$R_{G(int)}$	Internal Gate Resistance	—	0.73	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	V_{DD} = 39V
t_r	Rise Time	—	35	—		I_D = 47A
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		R_G = 10Ω
t_f	Fall Time	—	46	—		V_{GS} = 10V ④
C_{iss}	Input Capacitance	—	2290	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	270	—		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	—	130	—	pF	f = 1.0MHz
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)⑥	—	390	—		V_{GS} = 0V, V_{DS} = 0V to 60V ⑥
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)⑤	—	630	—		V_{GS} = 0V, V_{DS} = 0V to 60V ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	79	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	315		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 47A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	26	39	ns	T_J = 25°C V_R = 51V,
		—	31	47		T_J = 125°C I_F = 47A
Q_{rr}	Reverse Recovery Charge	—	24	36	nC	T_J = 25°C di/dt = 100A/µs ④
		—	35	53		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	1.8	—	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.08mH R_G = 25Ω, I_{AS} = 47A, V_{GS} =10V. Part not recommended for use above this value.

③ I_{SD} ≤ 47A, di/dt ≤ 1668A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

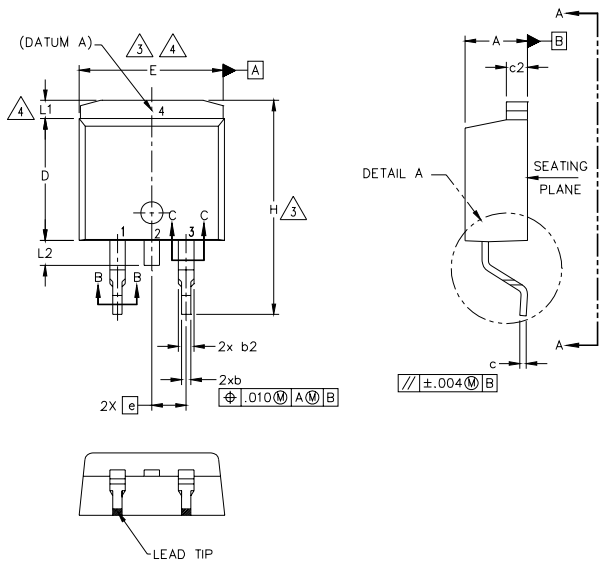
⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑧ R_θ is measured at T_J approximately 90°C.

⑨ This is only applied to TO-220

D²Pak Package Outline (Dimensions are shown in millimeters (inches))



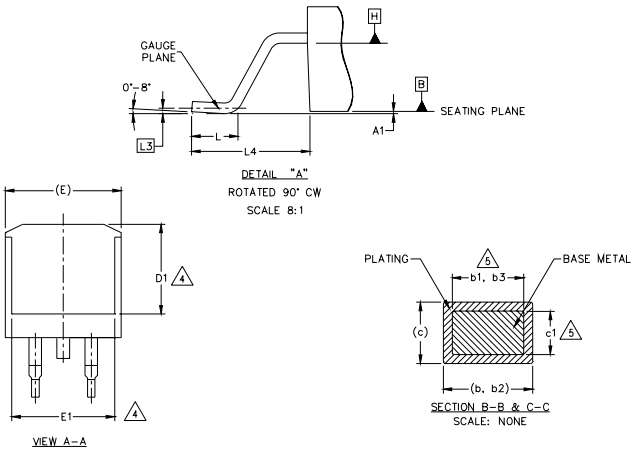
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.65	–	.066	4
L2	1.27	1.78	–	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

DIODES

1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

HEXFET	IGBTs, CoPACK
1.– GATE	1.– GATE
2, 4.– DRAIN	2, 4.– COLLECTOR
3.– SOURCE	3.– EMITTER

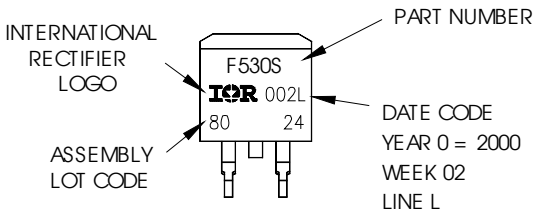


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"



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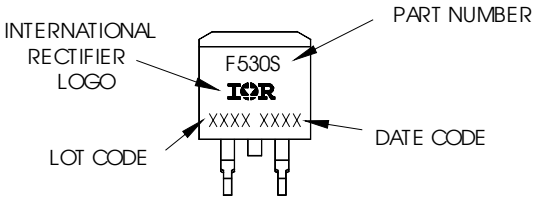
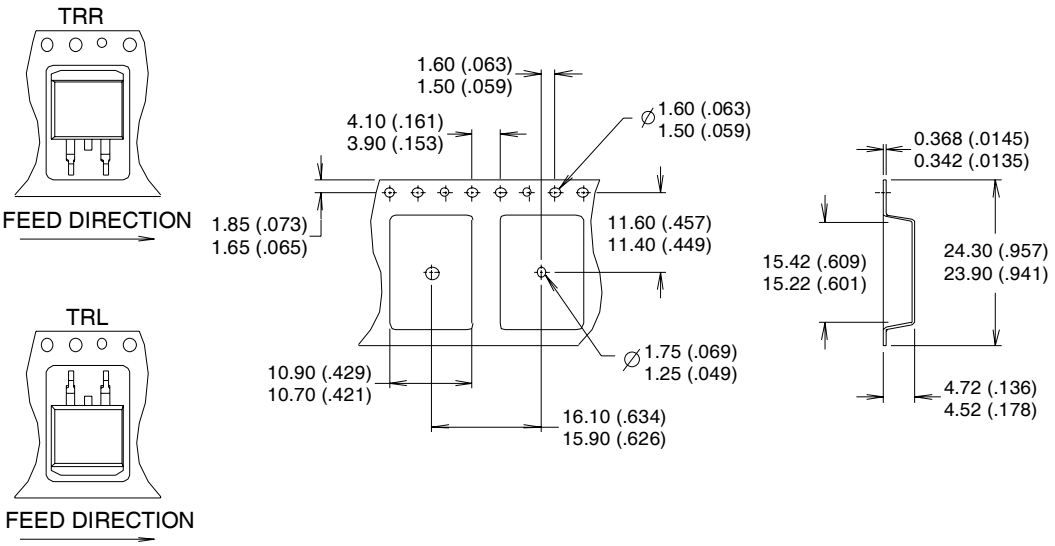
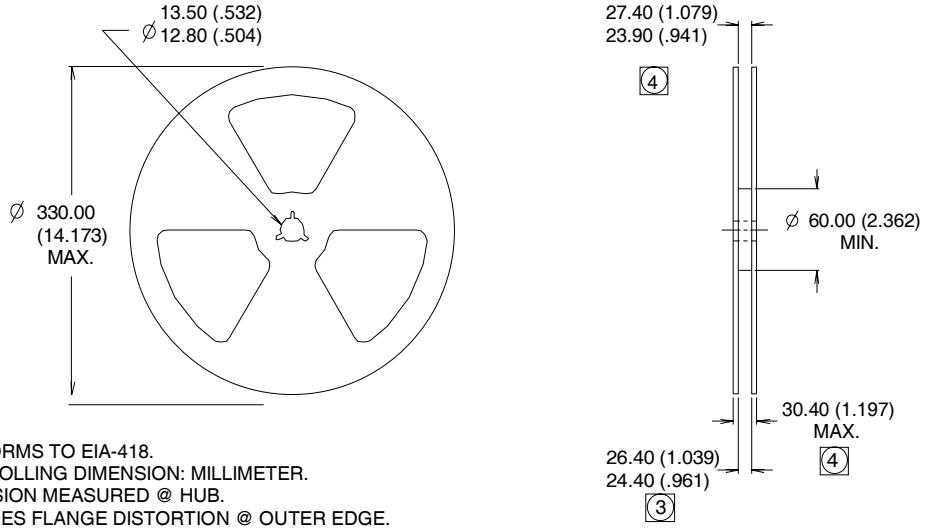


D²Pak Tape & Reel Information





NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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